Listing of Claims:

1. (Currently Amended) A circuit for a memory module address bus comprising:

a transmission line comprising a dampening impedance between a driver and a branch point of said transmission line; and

a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver;

said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

2. (Original) The circuit of Claim 1, wherein said transmission line is uni-directional.

3. (Original) The circuit of Claim 1, wherein said ones of said branches are coupled to two memory module interfaces.

4. (Original) The circuit of Claim 1, wherein said ones of said branches are coupled to three memory module interfaces.

5. (Original) The circuit of Claim 1, wherein said ones of said branches are coupled to four memory module interfaces.

6. (Currently Amended) The circuit of Claim 1, wherein the distance from said branch point to said one end of said parallel termination impedance is greater than the length of said branches.

7. (Currently Amended) The circuit of Claim 1, wherein said one end of said parallel termination impedance is connected to said series dampening impedance.

8. (Currently Amended) A circuit for reducing skew when addressing a memory module comprising:

a plurality of memory modules;

an address line coupling said memory modules;

a transmission line having a series dampening impedance and a parallel termination impedance in a stub configuration, wherein said parallel termination impedance is on the same side of any memory module as a driver; and

said transmission line having a first end coupled to ~~a~~ said driver and a second end connected at a point on said address line to reduce skew when addressing a memory module.

9. (Original) The circuit of Claim 8, wherein said second end of said transmission line is connected at substantially the midpoint of said address line.

10. (Original) The circuit of Claim 8, wherein said transmission line is uni-directional.

11. (Currently Amended) The circuit of Claim 8, wherein said parallel termination impedance is connected to said series dampening impedance.

12. (Original) The circuit of Claim 8, wherein said plurality of memory modules is an odd number and wherein said second end of said transmission line is connected to said address line at the middle memory module.

13. (Original) The circuit of Claim 8, wherein said plurality of memory modules is an even number and wherein said second end of said transmission line is connected to said address line at a point substantially midway between two memory modules closest to the mid-point of said address line.

14. (Currently Amended) A system for addressing memory modules comprising:

a bus controller;

a transmission line comprising a series dampening impedance between a driver and a branch point of said transmission line; and

a parallel termination impedance having a first end coupled to said transmission line between said series dampening impedance and said branch point and a second end coupled to a

termination voltage terminal, wherein said parallel termination impedance is one the same side of any memory module as a driver;

said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

15. (Original) The system of Claim 14, wherein two branches of said branches from said branch point have substantially the same length.

16. (Original) The system of Claim 14, wherein said transmission line is uni-directional.

17. (Original) The circuit of Claim 14, wherein said ones of said branches are coupled to two memory module interfaces.

18. (Original) The system of Claim 14, wherein said ones of said branches are coupled to three memory module interfaces.

19. (Original) The system of Claim 14, wherein said ones of said branches are coupled to four memory module interfaces.

20. (Currently amended) The system of Claim 14, wherein the distance from said branch point to said first end of said parallel termination impedance is greater than the length of said branches.

21. (Currently Amended) The system of Claim 14, wherein said first end of said parallel termination impedance is connected to said series dampening impedance.

22. (Currently Amended) The system of Claim 14, wherein said parallel termination impedance and said series dampening resistance are mounted on opposite sides of a printed circuit board.